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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Hiroshi Hatae

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8728

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05/05/2006

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EXAMINER

LI, AIMEE J

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/080,578		HATAE ET AL.	
	Examiner		Art Unit	
	Aimee J. Li		2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 18-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 18-26 is/are rejected.
- 7) ☒ Claim(s) 25 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-5, 18-24, and new claims 25-26 have been considered. Claims 1, 4-5, and 23 have been amended as per Applicant's request. New claims 25-26 have been added as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as filed 08 March 2006; Extension of Time for 3 Months as filed 08 March 2006; and Amendment as received on 08 March 2006.

Claim Objections

3. Claim 25 is objected to because of the following informalities: Please correct line 6 from "interpretation results of the SID command" to read --interpretation results of the [[SID]]SIMD command--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-5 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove et al., U.S. Patent Number 5,212,777 (herein referred to as Gove) in view of Wise, U.S. Patent Number 5,978,592 (herein referred to as Wise).

6. Referring to claim 1, Gove has taught a semiconductor integrated circuit, comprising:

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- a. A central processing unit conducting a single instruction multiple data (SIMD) command (Gove column 1, line 50 to column 2, line 5; column 3, lines 5-13; column 5, lines 20-47; column 6, lines 6-12; Figure 1; and Figure 2);
- b. A single instruction multiple data (SIMD) unit controlled by the central processing unit and including a plurality of operation units conducting a concurrent operation of data items for a plurality of data items respectively fetched therein in accordance with an interpretation result of said SIMD command by said processing unit (Gove column 1, line 50 to column 2, line 5; column 3, lines 5-13; column 5, lines 20-47; column 6, lines 6-12; Figure 1; and Figure 2);
- c. A data buffer connectible to said SIMD unit (Gove column 5, lines 20-47; column 6, lines 23-36; column 16, lines 6-17; Figure 1; Figure 2; and Figure 16); and
- d. A data transfer control unit for controlling transfer of data for said data buffer (Gove column 2, lines 47-53; column 2, line 62 to column 3, line 13; column 5, lines 35-48; column 12, lines 32-56; column 16, lines 6-17; Figure 1; Figure 2; Figure 17; and Figure 57),
- e. Wherein said data transfer control unit controls the transfer of data for a subsequent operation to said data buffer in concurrence with the operation of said SIMD unit for the plural data items read from said data buffer (Gove column 2, lines 47-53; column 2, line 62 to column 3, line 13; column 5, lines 35-48; column 12, lines 32-56; column 16, lines 6-17; Figure 1; Figure 2; Figure 17; and Figure 57). In regards to Gove, Gove has taught that the transfer processor is

autonomous from the SIMD processing area and feeds data into data buffer locations that are not in use by the SIMD.

7. Gove has not taught wherein said data transfer control unit controls transfer of data for a subsequent operation to said data buffer from a memory in concurrence with the current operation for a plurality of data items read from said data buffer. Wise has taught wherein said data transfer control unit controls transfer of data for a subsequent operation to said data buffer from outside of said semiconductor integrated circuit in concurrence with the current operation for a plurality of data items read from said data buffer (Wise column 248, lines 44-53; column 249, lines 1-6; Figure 24; and Figure 131). A person of ordinary skill in the art at the time the invention was made would have recognized that having a double buffer allows data to be read and written at the same time from the buffering area, thereby increasing processor speed, since read and write operations are done concurrently. Therefore, it would have been obvious to a person of ordinary skill in the art the time the invention was made to incorporate the double buffer of Wise in the device of Gove to increase processor speed.

8. Referring to claim 2, Gove in view of Wise has taught wherein said data buffer includes a dual-port unit including a first port and a second port (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; Figure 1; Figure 2; Figure 4; Figure 17; and Figure 57),

- a. Said first port being connected via a first bus to said SIMD unit (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 37, lines 5-20; Figure 1; Figure 2; Figure 4; Figure 17; Figure 30; and Figure 57),

- b. Said second port being connected via a second bus to said data transfer control unit (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 59, line 45 to column 60, line 3; Figure 1; Figure 2; Figure 4; Figure 17; and Figure 57). In regards to Gove, the port is inherent to the Transfer Processor in order for it to receive and transmit data.
- 9. Referring to claim 3, Gove in view of Wise has taught
 - a. Said first port concurrently input and output the plurality of data items for said first bus (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 37, lines 5-20; Figure 1; Figure 2; Figure 4; Figure 17; Figure 30; and Figure 57); and
 - b. Said second port concurrently input and output the plurality of data items for said second bus (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 59, line 45 to column 60, line 3; Figure 1; Figure 2; Figure 4; Figure 17; and Figure 57).
- 10. Referring to claim 4, Gove in view of Wise has taught
 - a. A first data register connected to said first bus, said first data register being concurrently latched the plurality of data items (Gove column 38, lines 9-12; column 39, lines 11-35; Figure 30; and Figure 32);
 - b. A second data register connected to said first bus, said second data register being concurrently latched the plurality of data items (Gove column 38, lines 9-12; column 39, lines 11-35; Figure 30; and Figure 32);

- c. Wherein said plurality of operation units receive the plurality of data items respectively latched by said first and second data registers and for conducting a concurrent operation for the data items (Gove column 38, lines 9-12; column 39, lines 11-35; Figure 30; and Figure 32).

11. Referring to claim 5, Gove in view of Wise has taught wherein said central processing unit conducting operation control for said SIMD unit and access control via said first bus to said data buffer (Gove column 5, lines 35-47; column 6, lines 23-25; column 12, line 59 to column 13, line 9; column 35, lines 36-49; Figure 1; Figure 2; Figure 4; Figure 17; Figure 29; and Figure 67).

12. Referring to claim 18, Gove has not taught wherein said data transfer control unit includes a bit extension unit for conducting bit extension for each of said plurality of data items transferred via said second bus to said data buffer. Wise has taught wherein said data transfer control unit includes a bit extension unit for conducting bit extension for each of said plurality of data items transferred via said second bus to said data buffer (Wise column 27, lines 42-53 and column 54, line 66 to column 55, line 5). A person of ordinary skill in the art, and as taught by Wise, would have recognized that all these traits improve the flexibility, efficiency and performance of a graphics processing system using video compression/decompression (Wise column 6, lines 8-13). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the bit extension and double buffering of Wise in the device of Gove to improve the flexibility, efficiency and performance.

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13. Referring to claim 19, Gove in view of Wise has taught wherein said bit extension unit conducts 1-bit code extension according to a lower-most bit of said plurality of data items (Wise column 27, lines 42-53 and column 54, line 66 to column 55, line 5).

14. Referring to claim 20, Gove in view of Wise has taught wherein said bit extension unit conducts bit extension for said plurality of data items (Wise column 27, lines 42-53 and column 54, line 66 to column 55, line 5) in a concurrent fashion (Gove column 1, line 50 to column 2, line 5; column 4, lines 5-13; column 5, lines 20-47; column 6, lines 6-12; Figure 1; and Figure 2).

15. Referring to claim 21, Gove in view of Wise has taught a data aligner in a stage before said bit extension unit for said plurality of data items (Wise column 75, lines 11-15 and column 132, lines 36-43).

16. Referring to claim 22, Gove in view of Wise has taught wherein said data transfer control unit includes a bit removal unit for removing bits from each of said plurality of data items which are used from said data buffer and which are transferred via said second bus (Wise column 248, lines 44-53; column 249, lines 1-6; and Figure 131). In regards to Wise, reading data from the double buffer removes bits from the buffer.

17. Referring to claim 23, Gove in view of Wise has taught wherein said bit removal unit removes a higher-most bit from said plurality of data items (Wise column 248, lines 44-53; column 249, lines 1-6; and Figure 131). In regards to Wise, reading data from the double buffer removes bits from the buffer, including the higher-most bit.

18. Referring to claim 24, Gove in view of Wise has taught wherein said first and second data registers latch image data when being in compression processing of image data (Wise

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column 36, line 57 to column 37, line 5 and Figure 19), and wherein said first data register latches image data and said second data register latches data of inverse discrete cosine transform (IDCT) when being in expansion of image data (Wise column 36, line 57 to column 37, line 5; column 74, lines 60-67; and Figure 19).

19. Referring to claim 25, Gove has taught a semiconductor integrated circuit on semiconductor chip, the semiconductor integrated circuit comprising:

- a. A CPU executing a single instruction multiple data (SIMD) command (Gove column 1, line 50 to column 2, line 5; column 3, lines 5-13; column 5, lines 20-47; column 6, lines 6-12; Figure 1; and Figure 2);
- b. A SIMD unit including operation unit which concurrently execute operations of first data items fetched in the respective operation units in accordance with interpretation results of the SIMD command by the CPU (Gove column 1, line 50 to column 2, line 5; column 3, lines 5-13; column 5, lines 20-47; column 6, lines 6-12; Figure 1; and Figure 2);
- c. A data buffer having:
 - i. A first port coupled to the operation units in the SIMD unit and providing the first data items to the operation units in the SIMD unit under control of the CPU (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 37, lines 5-20; Figure 1; Figure 2; Figure 4; Figure 17; Figure 30; and Figure 57), and

- ii. A second port (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 37, lines 5-20; Figure 1; Figure 2; Figure 4; Figure 17; Figure 30; and Figure 57);
- 20. Gove has not taught
 - a. A data transfer control unit coupled to the second port of the data buffer and controlling a transfer of the first data items to the second port of the data buffer, the data transfer control unit including:
 - i. First data aligners having inputs coupled to receive second data items from a memory and each having a bit shift function in 8 bits unit to a high-order side or a lower-order side to align the second data items for the operation units in the SIMD unit; and
 - ii. Bit extension units coupled to the second port of the data buffer and coupled to receive the aligned second data items and providing the first data items by adding a sign bit to each of the aligned second data items,
 - b. Wherein the data transfer control unit provides the next first data items to the data buffer unit for a subsequent operation of the SIMD unit, while executing the current first data items by the operation unit in the SIMD unit.
- 21. Wise has taught wherein
 - a. A data transfer control unit coupled to the second port of the data buffer and controlling a transfer of the first data items to the second port of the data buffer (Wise column 27, lines 42-53 and column 54, line 66 to column 55, line 5), the data transfer control unit including:

- i. First data aligners having inputs coupled to receive second data items from a memory and each having a bit shift function in 8 bits unit to a high-order side or a lower-order side to align the second data items for the operation units in the SIMD unit (Wise column 75, lines 11-15 and column 132, lines 36-43); and
 - ii. Bit extension units coupled to the second port of the data buffer and coupled to receive the aligned second data items and providing the first data items by adding a sign bit to each of the aligned second data items (Wise column 27, lines 42-53 and column 54, line 66 to column 55, line 5),
- b. Wherein the data transfer control unit provides the next first data items to the data buffer unit for a subsequent operation of the SIMD unit, while executing the current first data items by the operation unit in the SIMD unit (Wise column 248, lines 44-53; column 249, lines 1-6; Figure 24; and Figure 131).

22. A person of ordinary skill in the art, and as taught by Wise, would have recognized that all these traits improve the flexibility, efficiency and performance of a graphics processing system using video compression/decompression (Wise column 6, lines 8-13). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the bit extension and double buffering of Wise in the device of Gove to improve the flexibility, efficiency and performance.

23. Referring to claim 26, Gove in view of Wise has taught wherein the data transfer control unit further comprises:

- a. Second data aligners having inputs coupled to the second port of the data buffer and each having a bit shift function in 8 bits unit to a high-order side or a lower-order side to align the third data items from the data buffer, the third data items being provided from the operation units in the unit as operation results of the first data items (Wise column 75, lines 11-15 and column 132, lines 36-43); and
- b. Bit removal units having inputs coupled to receive the aligned third data items and providing fourth data items to be provided to the memory by removing a sign bit from each of the third data items (Wise column 248, lines 44-53; column 249, lines 1-6; and Figure 131).

Response to Arguments

24. Applicant's arguments filed 08 March 2006 have been fully considered but they are not persuasive. Applicant argues in essence on pages 8-13

The Examiner's reliance upon the 'common knowledge and common sense' of one skilled in the art for the motivation for combining the teachings Wise with Gove did not fulfill the agency's obligation to cite references to support its conclusions. Instead, the Examiner must provide the specific teaching of allegation of the combination on the record to allow accountability.

25. This has not been found persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

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See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to combine was that the double buffering and bit extension of Wise improve the flexibility, efficiency, and performance of the system. This is not only obvious to a person of ordinary skill in the art, but it is also taught by Wise. Wise in column 6, lines 8-13 states that his invention, which uses double buffering and bit extension, enhances flexibility, efficiency and performance of a system. Wise further teaches in column 249, lines 36-41 that a double buffering system transfers data "...at least as fast as the sum of all the average data rates between the swing buffer and the rest of the chip", e.g. the double buffering system improves the transfer rate, thereby improving the performance speed of the system. Also, Wise teaches in column 250, lines 17-26 "...the amount of DRAM used can be matched to the size and bandwidth requirements of the particular application" e.g. improving the flexibility and efficiency of a system by customizing the use of DRAM to a particular process. Therefore, while the Examiner did rely upon "common knowledge and common sense" of one skilled in the art, this "common knowledge and common sense" was also supported by the teachings in Wise.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
25 April 2006



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